REMARKS

Claims 1-12 remain pending.

It is believed that this Amendment is fully responsive to the Office Action dated **March 15, 2002**.

In the Title:

In the outstanding Office action. The Office has stated that "The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed."

Accordingly, a new title "A Semiconductor Device with More Than One Impurity Region" is submitted herein. Should the Office feel this title is insufficient, the Undersigned welcomes any Office suggestions.

Rejection Under 35 U.S.C. §102(e):

Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by **Arita et al. (US 6,046,490)**.

The outstanding Office action has positively stated that:

> "Ants shows (fig. 1) a semiconductor device comprising a transistor having a first and second impurity region (3) formed in a substrate (1), and a gate electrode (5). A first insulating layer (6) covers the transistor. A capacitor (10) is formed on the insulating layer, the capacitor having a dielectric (8) formed of a high dielectric constant material (ccl. 8, lines 3945), and an upper electrode (9) and lower electrode (7) with the dielectric positioned therebetween. A silicon oxide film (22) is formed

over the capacitor and has its upper surface planarized. The upper surface of the oxide includes nitrogen because a silicon nitride film (14) is formed on the oxide. A second insulating film (15) is formed between the capacitor and the silicon oxide film."

The Applicant respectfully disagrees with this Office position. In claim 1, nitrogen is introduced all over the surface of the silicon oxide film. Consequently, it is able to keep moisture from entering into the silicon oxide film.

Regarding Arita, as explained in the outstanding Office action, the silicon oxide (22) has been positively cited to be correspondent to a silicon oxide of the claimed invention. As clearly shown in Figure 1 of Arita, on the silicon oxide (22), a passivation layer (14) is formed.

Though the Examiner asserts that the upper surface of the oxide includes nitrogen because a passivation layer (14) is formed on the oxide, the claimed invention is not anticipated because in Arita, nitrogen is not included in the upper surface of the oxide directly under wirings (19a), (19b) and the insulating layer (21). Therefore, the passivation layer 14 cannot protect moisture from coming into contact with either wirings (19a), (19b) or the insulating layer (21).

However, the present invention is able to prevent moisture from entering into the silicon oxide thereby preventing formation of any film on the silicon oxide, for instance, any silicon nitride film.

Since the claimed invention does not form such a silicon nitride film, the manufacturing process is greatly simplified.

To further define features of the present invention, independent claim 1 has been further amended as shown hereinbelow:

"1. (Amended) A semiconductor device comprising;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film for covering the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween; and

a silicon oxide film placed over the capacitor forming a planarized surface; wherein nitrogen being introduced all over the planarized surface of the silicon oxide film."

It is well settled that:

"A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office believe that independent claim 1, as amended, is anticipated by Arita, a citation of where each and every element of the claimed invention is disclosed in Arita is respectfully requested.

It is respectfully submitted that independent claim 1, as amended, patentably distinguishes over Arita. All claims dependent thereon, by virtue of inherency, also patentably distinguish over Arita. Reconsideration and withdrawal of this rejection are respectfully requested.

Claims 5, 9, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by **Mochizuki et al. (US 5,990,507)**.

The outstanding Office action has positively stated that:

"Mochizuki et al. shows (fig. 17) a semiconductor device comprising

> a transistor having a first and second impurity region (S, 0) formed in a substrate (1), and a gate electrode (G, 4 & 5). A first insulating layer (10) covers the transistor. A capacitor is formed on the insulating layer, the capacitor having a dielectric (18) formed of a ferroelectnic material, and an upper electrode (19) and lower electrode (17) with the dielectric positioned therebetween. A second insulating film (13) is formed on the capacitor. A local interconnection (22) is formed on the second insulating film for connecting the upper electrode of the capacitor to the first impurity region (5). Third insulating film (30) is formed on the local interconnection and the second insulating film. A first wiring (BL) is formed on the third insulating film and electrically connects to the second impurity region (D)via a hole which is formed in the first, second, and third insulating films. A fourth insulating film (39) is formed on the first wiring and has a planarized upper surface. The upper surface of the first insulating film is planarized. A second wiring is formed on the fourth film and connects to the first wiring via a hole formed through the fourth insulating layer (col. 24, lines 49-67). The upper surface of the first insulating film is planarized."

The Applicant respectfully disagrees with the Office position. In claim 5, nitrogen is introduced all over the surface of the silicon oxide film. Consequently, it is able to keep moisture from entering into the silicon oxide film.

Regarding Mochizuki, as explained in the outstanding Office action, a second layer flattening interlayer insulation film (13) has been positively cited to be correspondent to a silicon oxide film of the claimed invention. As clearly shown in Figure 17 of Mochizuki, on the first interlayer insulation film (10), the second layer flattening interlayer insulation film (13) is formed.

Though the Examiner may have regarded that the first interlayer insulation film (10) includes nitrogen because the second layer flattening interlayer insulation film (13) formed thereon, the claimed invention is not anticipated because in Mochizuki, nitrogen is not included in the first interlayer insulation film (10) directly under contact plugs (33), (34). Therefore, the second layer

flattening interlayer insulation film (13) cannot protect moisture from coming into contact plugs (33), (34).

However, the present invention is able to prevent moisture from entering into the silicon oxide thereby preventing formation of any film on the silicon oxide, for instance, any silicon nitride film.

Since the claimed invention does not form such a silicon nitride film, the manufacturing process is greatly simplified.

To further define features of the present invention, independent claim 5 has been further amended as shown hereinbelow:

> "5. (Amended) A semiconductor device comprising;
> a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;
> a first insulating film for covering the transistor;
> a capacitor formed on the first insulating film, the capacitor having a dielectric formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;
> a second insulating film formed on the capacitor;
> a local interconnection formed on the second insulating film, for electrically connecting the upper electrode of the capacitor to the first impurity region;
> a third insulating film formed on the local interconnection and the second insulating film;
> a first wiring formed on the third insulating film and electrically connected to the second impurity region via a hole which is formed on the first insulating film, the second insulating film, and the third insulating film;
> a fourth insulating film placed on the first wiring forming an upper planarized surface,
> wherein nitrogen being introduced all over the upper planarized surface of the fourth insulating film; and
> a second wiring formed on the fourth insulating film."

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office believe that independent claim 5, as amended, is anticipated by Mochizuki, a citation of where each and every element of the claimed invention is disclosed in Mochizuki is respectfully requested.

It is respectfully submitted that independent claim 5, as amended, patentably distinguishes over Mochizuki. All claims dependent thereon, by virtue of inherency, also patentably distinguish over Mochizuki. Reconsideration and withdrawal of this rejection are respectfully requested.

Rejection Under 35 U.S.C. §103(a):

Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Arita et al. (US 6,046,490)** as applied to claim 1 above, and further in view of **Singh et al. (US 5,847,464)**.

As has been mentioned hereinabove that independent claim 1, as amended, patentably distinguishes over Arita. All claims dependent thereon, by virtue of inherency, also patentably distinguish over Arita further in view of whatever other references. Therefore, reconsideration and withdrawal of this rejection are respectfully requested.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Mochizuki et al. (US 5,990,507)**, as applied to claim 5 above, and further in view of **Singh et al. (US 5,847,464)**.

As has been mention hereinabove that independent claim 5, as amended, patentably distinguishes over Mochizuki. All claims dependent thereon, by virtue of inherency, also patentably distinguish over Mochizuki further in view of whatever other references. Therefore, reconsideration and withdrawal of this rejection are respectfully requested.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Mochizuki et al. (US 5,990,507)**, as applied to claim 5 above, and further in view of **Arita et al. (US 6,046,490)**.

As has been mention hereinabove that independent claim 5, as amended, patentably distinguishes over Mochizuki. All claims dependent thereon, by virtue of inherency, also patentably distinguish over Mochizuki further in view of whatever other references. Therefore, reconsideration and withdrawal of this rejection.

Claim 12 is rejected under 35 U.S.C. 102(e) as being anticipated by **Arita et al. (US 6,046,490)**.

The outstanding Office action has positively stated that:

> "Anita shows (fig. 1) a semiconductor device comprising a transistor having a first and second impurity region (3) formed in a substrate (1), and a gate electrode (5). A first insulating layer (6) covers the transistor. A capacitor (10) is formed on the insulating layer, the capacitor having a dielectric (8) formed of a high dielectric constant material (col. 8, lines 39-45), and an upper electrode (9) and lower electrode (7) with the dielectric positioned therebetween. A silicon oxide film (22) is formed over the capacitor and has its upper surface planarized. The upper surface of the oxide includes nitrogen because a silicon nitride film (14) is formed on the oxide. A second insulating film (15) is formed between the capacitor and the silicon oxide film.
>
> With respect to the limitation of claim 12 concerning the insulating layer

being plasma annealed, a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17(footnote 3). See also in re Brown, 173 USPQ 685: In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324: In re Avery, 186 USPQ 116 in re Wertheim, 191 USPQ 90 (209 USPQ 254 does not deal with this issue); and In re Marosi et aI, 218 USPQ 289 final product per se which must be determined in a "product by, all or claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted)."

The Applicant respectfully disagrees with this Office position. In claim 12, nitrogen is introduced all over the surface of the silicon oxide film. Consequently, it is able to keep moisture from entering into the silicon oxide film.

Regarding Arita, as explained in the outstanding Office action, the silicon oxide (22) has been positively cited to be correspondent to a silicon oxide of the claimed invention. As clearly shown in Figure 1 of Arita, on the silicon oxide (22), a passivation layer (14) is formed.

Though the Examiner asserts that the upper surface of the oxide includes nitrogen because a passivation layer (14) is formed on the oxide, the claimed invention is not anticipated because in Arita, nitrogen is not included in the upper surface of the oxide directly under wirings (19a), (19b) and the insulating layer (21). Therefore, the passivation layer 14 cannot protect moisture from coming into contact with either wirings (19a), (19b) or the insulating layer (21).

However, the present invention is able to prevent moisture from entering into the silicon oxide thereby preventing formation of any film on the silicon oxide, for instance, any silicon nitride

film.

Since the claimed invention does not form such a silicon nitride film, the manufacturing process is greatly simplified.

To further define features of the present invention, independent claim 12 has been further amended as shown hereinbelow:

> "12. (Amended) a semiconductor device comprising:
> a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;
> a first insulating film for covering the transistor;
> a capacitor formed on the first insulating film, the capacitor having a dielectric film formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;
> a second insulating film covering the capacitor to become an upper planarized surface; and
> wherein a surface of the second insulating film is planarized and nitrogen is introduced by plasma processing all over the upper planarized surface of the second insulating film."

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office believe that independent claim 12, as amended, is anticipated by Arita, a citation of where each and every element of the claimed invention is disclosed in Arita is respectfully requested.

It is respectfully submitted that independent claim 12, as amended, patentably distinguishes over Arita. Reconsideration and withdrawal of this rejection are respectfully requested.

Prior Art Indicated to be Pertinent to the Disclosure

The Office has provided a list of prior art indicated to be pertinent to the Applicant's invention. Consistent with the understanding as stipulated in MPEP 706.02 that only the best prior art should be applied, this list of prior art not having been applied by the Office, naturally, the Office must have considered them to be no more pertinent than the applied prior art of record.

CONCLUSION

In view of the aforementioned amendments and accompanying remarks, all pending claims are believed to be in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

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Enclosures: Version with markings to show changes made

VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/594,091

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A semiconductor device comprising;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film for covering the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween; and

a silicon oxide film ~~formed~~ placed over the capacitor ~~and having its~~ forming a planarized surface~~;~~ ; ~~at least the planarized surface on the silicon oxide film including nitrogen.~~

wherein nitrogen being introduced all over the planarized surface of the silicon oxide film.

5. (Amended) A semiconductor device comprising;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film for covering the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film formed on the capacitor;

a local interconnection formed on the second insulating film, for electrically connecting the upper electrode of the capacitor to the first impurity region;

a third insulating film formed on the local interconnection and the second insulating film;

a first wiring formed on the third insulating film and electrically connected to the second impurity region via a hole which is formed on the first insulating film, the second insulating film, and the third insulating film;

a fourth insulating film ~~formed~~ placed on the first wiring ~~and having its~~ forming an upper planarized surface,

wherein nitrogen being introduced all over the upper planarized surface of the fourth insulating film; and

a second wiring formed on the fourth insulating film.

12. (Amended) a semiconductor device comprising:

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film for covering the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film covering the capacitor to become an upper planarized surface; and

wherein a surface of the second insulating film is planarized and ~~plasma annealed~~ nitrogen is introduced by plasma processing all over the upper planarized surface of the second insulating film.